

# LMx24, LMx24x, LMx24xx, LM2902, LM2902x, LM2902xx, LM2902xxx

## Quadruple Operational Amplifiers

### 1 Features

- Wide supply range:
  - 3 V to 36 V (B, BA versions)
  - 3 V to 30 V (LMx24, LM2902V)
- Low input offset voltage maximum at 25°C:
  - 2 mV (BA versions LM2902A, LM124A)
  - 3 mV (B versions LMx24xA)
- Low input bias current maximum at 25°C:
  - 35 nA (B, BA versions)
- 2-kV ESD protection (HBM) (B, BA, K versions)
- Internal RF and EMI filter (B, BA versions)
- Low quiescent current of 175- $\mu$ A/ch typical
- Common-mode input voltage range includes  $V_{CC-}$
- Differential input voltage range equal to maximum-rated supply voltage
- Open-loop differential voltage amplification: 100-V/mV typical
- On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

### 2 Applications

- Merchant network and server power supply units
- Multi-function printers
- Power supplies and mobile chargers
- Motor control: AC induction, brushed DC, brushless DC, high-voltage, low-voltage, permanent magnet, and stepper motor
- Desktop PC and motherboard
- Indoor and outdoor air conditioners
- Washers, dryers, and refrigerators
- AC inverters, string inverters, central inverters, and voltage frequency drives
- Uninterruptible power supplies

- Electronic point-of-sale systems

### 3 Description

These devices consist of four independent, high-gain, frequency-compensated, operational amplifiers that are designed specifically to operate from a single supply or split supply over a wide range of voltages.

#### Device Information

PART NUMBER <sup>(1)</sup>	PACKAGE	BODY SIZE (NOM)
LM324B <sup>(2)</sup> , LM324BA <sup>(2)</sup> , LM2902B <sup>(2)</sup> , LM2902BA <sup>(2)</sup> , LM324, LM324A, LM324K, LM324KA, LM2902, LM2902K, LM2902KV, LM2902KAV, LM224, LM224A, LM224K, LM224KA, LM124	SOIC (14)	8.65 mm × 3.91 mm
LM324B <sup>(2)</sup> , LM324BA <sup>(2)</sup> , LM2902B <sup>(2)</sup> , LM2902BA <sup>(2)</sup> , LM324, LM324A, LM324K, LM324KA, LM2902, LM2902K, LM2902KV, LM2902KAV, LM124	TSSOP (14)	5.00 mm × 4.40 mm
LM324, LM324A, LM324K, LM324KA, LM2902, LM2902K, LM224, LM224A, LM224K, LM224KA	PDIP (14)	19.30 mm × 6.35 mm
LM324, LM324A, LM324K, LM324KA, LM2902, LM2902K	SO (14)	9.20 mm × 5.30 mm
LM324A, LM2902K	SSOP (14)	6.20 mm × 5.30 mm
LM124A	CDIP (14)	19.56 mm × 6.67 mm
	CFP (14)	9.21 mm × 5.97 mm
	LCCC (20)	8.90 mm × 8.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) This product is preview only.

### Family Comparison

SPECIFICATION	LM324B LM324BA	LM2902B LM2902BA	LM324 LM324A	LM324K LM324KA	LM2902	LM2902K LM2902KV LM2902KAV	LM224 LM224A	LM224K LM224KA	LM124 LM124A	Units
Supply voltage	3 to 36	3 to 36	3 to 30	3 to 30	3 to 26	3 to 26 3 to 30 3 to 30	3 to 30	3 to 30	3 to 30	V
Offset voltage (max, 25°C)	$\pm 3$ $\pm 2$	$\pm 3$ $\pm 2$	$\pm 7$ $\pm 3$	$\pm 7$ $\pm 3$	$\pm 7$	$\pm 7$ $\pm 7$ $\pm 2$	$\pm 5$ $\pm 3$	$\pm 5$ $\pm 3$	$\pm 5$ $\pm 2$	mV
Input bias current (typ / max)	10 / 35	10 / 35	20 / 250 15 / 100	20 / 250 15 / 100	20 / 250	20 / 250	20 / 150 15 / 80	20 / 150 15 / 80	20 / 150 20 / 50	nA
ESD (HBM)	2000	2000	500	2000	500	2000	500	2000	500	V
Operating ambient temperature	-40 to 85	-40 to 125	0 to 70	0 to 70	-40 to 125	-40 to 125	-25 to 85	-25 to 85	-55 to 125	°C



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## 4 Revision History

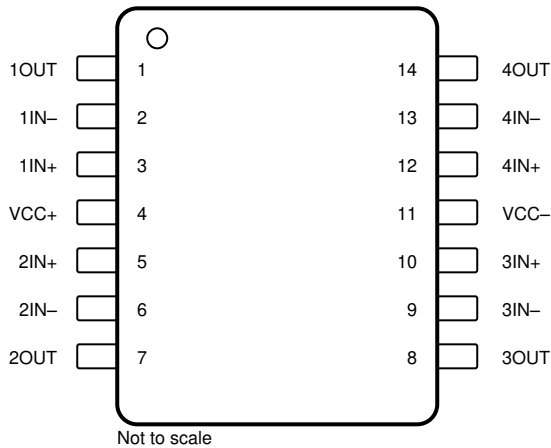
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision W (March 2015) to Revision X (May 2022)</b>	<b>Page</b>
• Updated <i>Features</i> to include the B and BA versions.....	1
• Added application links to <i>Applications</i> section.....	1
• Corrected available packages in the <i>Device Information</i> table.....	1
• Added B and BA versions to <i>Device Information</i> table.....	1
• Updated package images in the <i>Pin Configuration and Functions</i> section to new format - no specification changes.....	3
• Renamed GND and Vcc to Vcc- and Vcc+, respectively, in the <i>Pin Functions</i> table .....	3
• Added B and BA versions to <i>Absolute Maximum Ratings</i> table .....	4
• Added the B and BA versions to the <i>ESD Ratings</i> table .....	4
• Added B and BA versions to <i>Recommended Operating Conditions</i> table .....	4
• Added the <i>Electrical Characteristics - LM324B and LM324BA</i> table .....	6
• Added the <i>Electrical Characteristics - LM2902B and LM2902BA</i> table.....	8
• Removed <i>Documentation Support</i> and <i>Related Links</i> in the <i>Device and Documentation Support</i> section.....	20

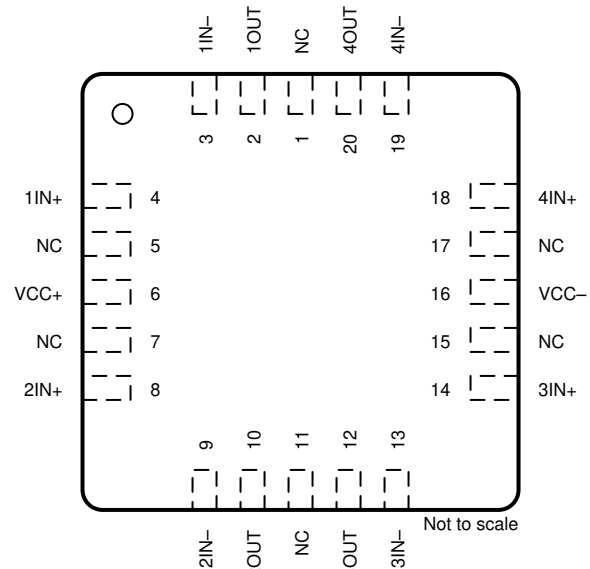
<b>Changes from Revision V (January 2014) to Revision W (March 2014)</b>	<b>Page</b>
• Added <i>Applications</i> .....	1
• Added <i>Device Information</i> table.....	1
• Added <i>Mechanical, Packaging, and Orderable Information</i> section.....	20

<b>Changes from Revision U (August 2010) to Revision V (January 2014)</b>	<b>Page</b>
• Updated document to new TI data sheet format - no specification changes.....	1
• Updated <i>Features</i> .....	1
• Removed <i>Ordering Information</i> table.....	3
• Added <i>Pin Functions</i> table .....	3

## 5 Pin Configuration and Functions



**Figure 5-1. D, DB, J, N, NS, PW, and W Package  
14-Pin SOIC, SSOP, CDIP, PDIP, SO, TSSOP, and  
CFP  
(Top View)**



**Figure 5-2. FK Package  
20-Pin LCCC  
(Top View)**

**Table 5-1. Pin Functions**

NAME	PIN		I/O	DESCRIPTION
	LCCC	SOIC, TSSOP, PDIP, SSOP, SO, CDIP, and CFP		
1IN-	3	2	I	Negative input
1IN+	4	3	I	Positive input
1OUT	2	1	O	Output
2IN-	9	6	I	Negative input
2IN+	8	5	I	Positive input
2OUT	10	7	O	Output
3IN-	13	9	I	Negative input
3IN+	14	10	I	Positive input
3OUT	12	8	O	Output
4IN-	19	13	I	Negative input
4IN+	18	12	I	Positive input
4OUT	20	14	O	Output
V <sub>CC-</sub>	16	11	—	Negative (lowest) supply or ground (for single-supply operation)
NC	1, 5, 7, 11, 15, 17	—	—	Do not connect
V <sub>CC+</sub>	6	4	—	Positive (highest) supply

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	LM324B, LM324BA, LM2902B, LM2902BA		LM2902		LM324xx, LM224xx, LM2902xxx, LM124x		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{CC}$ <sup>(2)</sup>	40		26		32		V
Differential input voltage, $V_{ID}$ <sup>(3)</sup>	±40		±26		±32		V
Input voltage, $V_I$ (either input)	-0.3	40	-0.3	26	-0.3	32	V
Duration of output short circuit (one amplifier) to ground at (or below) $T_A = 25^\circ\text{C}$ , $V_{CC} \leq 15\text{ V}$ <sup>(4)</sup>	Unlimited		Unlimited		Unlimited		
Operating virtual junction temperature, $T_J$	150		150		150		°C
Case temperature for 60 seconds	FK package				260		°C
Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds	J or W package		300		300		°C
Storage temperature, $T_{stg}$	-65	150	-65	150	-65	150	°C

- Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values (except differential voltages and  $V_{CC}$  specified for the measurement of  $I_{OS}$ ) are with respect to the network GND.
- Differential voltages are at  $IN+$ , with respect to  $IN-$ .
- Short circuits from outputs to  $V_{CC}$  can cause excessive heating and eventual destruction.

### 6.2 ESD Ratings

			VALUE	UNIT
<b>LM324B, LM324BA, LM2902B, LM2902BA, LM224K, LM224KA, LM324K, LM324KA, LM2902K, LM2902KV, LM2902KAV</b>				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	
<b>LM124, LM124A, LM224, LM224A, LM324, LM324A, LM2902</b>				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101	±1000	

- JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	LM324B, LM324BA, LM2902B, LM2902BA		LM2902		LM324xx, LM224xx, LM2902xxx, LM124x		UNIT	
	MIN	MAX	MIN	MAX	MIN	MAX		
$V_{CC}$ Supply voltage	3	36	3	26	3	30	V	
$V_{CM}$ Common-mode voltage	0	$V_{CC} - 2$	0	$V_{CC} - 2$	0	$V_{CC} - 2$	V	
$T_A$ Operating free air temperature	LM124x				-55	125	°C	
	LM2902xxx, LM2902Bx	-40	125	-40	125			
	LM324Bx	-40	85					
	LM224xx					-25		85
	LM324xx					0		70

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	LMx24, LM2902					LMx24			UNIT	
	D (SOIC)	DB (SSOP)	N (PDIP)	NS (SO)	PW (TSSOP)	FK (LCCC)	J (CDIP)	W (CFP)		
	14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	20 PINS	14 PINS	14 PINS		
R <sub>θJA</sub> <sup>(2) (3)</sup>	Junction-to-ambient thermal resistance	86	86	80	76	113	—	—	—	°C/W
R <sub>θJC</sub> <sup>(4)</sup>	Junction-to-case (top) thermal resistance	—	—	—	—	—	5.61	15.05	14.65	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Short circuits from outputs to VCC can cause excessive heating and eventual destruction.
- (3) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>)/R<sub>θJA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (4) Maximum power dissipation is a function of T<sub>J(max)</sub>, R<sub>θJA</sub>, and T<sub>C</sub>. The maximum allowable power dissipation at any allowable case temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>C</sub>)/R<sub>θJC</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.

## 6.5 Electrical Characteristics - LM324B and LM324BA

For  $V_S = (V_{CC+}) - (V_{CC-}) = 5\text{ V to }36\text{ V}$  ( $\pm 2.5\text{ V to } \pm 18\text{ V}$ ), at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>								
$V_{OS}$	Input offset voltage	LM324B				$\pm 0.3$	$\pm 3.0$	mV
			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		$\pm 4.0$			
		LM324BA				$\pm 0.3$	$\pm 2$	
			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		2.5			
$dV_{OS}/dT$	Input offset voltage drift	$R_S = 0\ \Omega$	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$			$\pm 7$		$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage versus power supply				65	100		dB
	Channel separation	$f = 1\text{ kHz to } 20\text{ kHz}$				120		dB
<b>INPUT VOLTAGE RANGE</b>								
$V_{CM}$	Common-mode voltage range	$V_S = 3\text{ V to } 36\text{ V}$			V-	$(V+) - 1.5$	V	
		$V_S = 5\text{ V to } 36\text{ V}$	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	V-	$(V+) - 2$			
CMRR	Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+) - 1.5\text{ V}$	$V_S = 3\text{ V to } 36\text{ V}$		70	80	dB	
		$(V-) \leq V_{CM} \leq (V+) - 2\text{ V}$	$V_S = 5\text{ V to } 36\text{ V}$	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	65	80		
<b>INPUT BIAS CURRENT</b>								
$I_B$	Input bias current				-10	-35	nA	
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$				-50		
$dI_{OS}/dT$	Input offset current drift	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$				10		$\text{pA}/^\circ\text{C}$
$I_{OS}$	Input offset current				$\pm 0.5$	$\pm 4$	nA	
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$				$\pm 5$		
$dI_{OS}/dT$	Input offset current drift	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$				10		$\text{pA}/^\circ\text{C}$
<b>NOISE</b>								
$E_N$	Input voltage noise	$f = 0.1\text{ to } 10\text{ Hz}$				3		$\mu\text{V}_{PP}$
$e_N$	Input voltage noise density	$R_S = 100\ \Omega, V_I = 0\text{ V}, f = 1\text{ kHz}$ (see Figure 8)				35		$\text{nV}/\sqrt{\text{Hz}}$
<b>INPUT CAPACITANCE</b>								
$Z_{ID}$	Differential					$10 \parallel 0.1$		$\text{M}\Omega \parallel \text{pF}$
$Z_{ICM}$	Common-mode					$4 \parallel 1.5$		$\text{G}\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>								
$A_{OL}$	Open-loop voltage gain	$V_S = 15\text{ V}, V_O = 1\text{ V to } 11\text{ V}, R_L \geq 2\text{ k}\Omega$ , connected to (V-)				50	100	V/mV
		$T_A = -40^\circ\text{C to } 85^\circ\text{C}$				25		
<b>FREQUENCY RESPONSE</b>								
GBW	Gain-bandwidth product	$R_L = 1\text{ M}\Omega, C_L = 20\text{ pF}$ (see Figure 7)				1.2		MHz
SR	Slew rate	$R_L = 1\text{ M}\Omega, C_L = 30\text{ pF}, V_I = \pm 10\text{ V}$ (see Figure 7)				0.5		V/ $\mu\text{s}$
$\theta_m$	Phase margin	$G = +1, R_L = 10\text{ k}\Omega, C_L = 20\text{ pF}$				56		$^\circ$
$t_s$	Settling time	To 0.1%, $V_S = 5\text{ V}, 2\text{-V Step}, G = +1, C_L = 100\text{ pF}$				4		$\mu\text{s}$
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$				10		$\mu\text{s}$
THD+N	Total harmonic distortion + noise	$G = +1, f = 1\text{ kHz}, V_O = 3.53\text{ }V_{RMS}, V_S = 36\text{ V}, R_L = 100\text{ k}\Omega, I_{OUT} \leq 50\ \mu\text{A}, \text{BW} = 80\text{ kHz}$				0.001%		
<b>OUTPUT</b>								
$V_O$	Voltage output swing from rail	Positive Rail (V+)		$I_{OUT} = -50\ \mu\text{A}$	1.35	1.5	V	
$V_O$				$I_{OUT} = -1\text{ mA}$	1.4	1.6	V	
$V_O$				$I_{OUT} = -5\text{ mA}$	1.5	1.75	V	
$V_O$		Negative Rail (V-)		$I_{OUT} = 50\ \mu\text{A}$	100	150	mV	
$V_O$				$I_{OUT} = 1\text{ mA}$	0.75	1	V	
$V_O$				$V_S = 5\text{ V}, R_L \leq 10\text{ k}\Omega$ connected to (V-)	$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	5	20	mV
$I_O$	Output current	$V_S = 15\text{ V}; V_O = V-; V_{ID} = 1\text{ V}$	Source		-20	-30	mA	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	-10		mA	
		$V_S = 15\text{ V}; V_O = V+; V_{ID} = -1\text{ V}$	Sink		10	20	mA	
				$T_A = -40^\circ\text{C to } 85^\circ\text{C}$	5		mA	
		$V_{ID} = -1\text{ V}; V_O = (V-) + 200\text{ mV}$			50	85	$\mu\text{A}$	
$I_{SC}$	Short-circuit current	$V_S = 20\text{ V}, (V+) = 10\text{ V}, (V-) = -10\text{ V}, V_O = 0\text{ V}$				$\pm 40$	$\pm 60$	mA
$C_{LOAD}$	Capacitive load drive					100		pF

## 6.5 Electrical Characteristics - LM324B and LM324BA (continued)

For  $V_S = (V_{CC+}) - (V_{CC-}) = 5\text{ V to }36\text{ V}$  ( $\pm 2.5\text{ V to } \pm 18\text{ V}$ ), at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{k}$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_O$	Open-loop output impedance	$f = 1\text{ MHz}, I_O = 0\text{ A}$			300		$\Omega$
<b>POWER SUPPLY</b>							
$I_Q$	Quiescent current per amplifier	$V_S = 5\text{ V}; I_O = 0\text{ A}$	$T_A = -40^\circ\text{C to }85^\circ\text{C}$		175	300	$\mu\text{A}$
		$V_S = 36\text{ V}; I_O = 0\text{ A}$	$T_A = -40^\circ\text{C to }85^\circ\text{C}$		350	750	$\mu\text{A}$

## 6.6 Electrical Characteristics - LM2902B and LM2902BA

For  $V_S = (V_{CC+}) - (V_{CC-}) = 5\text{ V to }36\text{ V}$  ( $\pm 2.5\text{ V to } \pm 18\text{ V}$ ), at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{ k}\Omega$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>OFFSET VOLTAGE</b>							
$V_{OS}$	Input offset voltage	LM2902B			$\pm 0.3$	$\pm 3.0$	mV
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$			$\pm 4.0$	
		LM2902BA			$\pm 0.3$	$\pm 2$	
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$			$2.5$	
$dV_{OS}/dT$	Input offset voltage drift	$R_S = 0\ \Omega$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		$\pm 7$		$\mu\text{V}/^\circ\text{C}$
PSRR	Input offset voltage versus power supply			65	100		dB
	Channel separation	$f = 1\text{ kHz to }20\text{ kHz}$			120		dB
<b>INPUT VOLTAGE RANGE</b>							
$V_{CM}$	Common-mode voltage range	$V_S = 3\text{ V to }36\text{ V}$		V-		$(V+) - 1.5$	V
		$V_S = 5\text{ V to }36\text{ V}$		$T_A = -40^\circ\text{C to }125^\circ\text{C}$	V-		
CMRR	Common-mode rejection ratio	$(V-) \leq V_{CM} \leq (V+) - 1.5\text{ V}$	$V_S = 3\text{ V to }36\text{ V}$		70	80	dB
		$(V-) \leq V_{CM} \leq (V+) - 2\text{ V}$	$V_S = 5\text{ V to }36\text{ V}$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$	65	80	
<b>INPUT BIAS CURRENT</b>							
$I_B$	Input bias current				-10	-35	nA
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$			-50	
$dI_{OS}/dT$	Input offset current drift		$T_A = -40^\circ\text{C to }125^\circ\text{C}$		10		$\text{pA}/^\circ\text{C}$
$I_{OS}$	Input offset current				$\pm 0.5$	$\pm 4$	nA
			$T_A = -40^\circ\text{C to }125^\circ\text{C}$			$\pm 5$	
$dI_{OS}/dT$	Input offset current drift		$T_A = -40^\circ\text{C to }125^\circ\text{C}$		10		$\text{pA}/^\circ\text{C}$
<b>NOISE</b>							
$E_N$	Input voltage noise	$f = 0.1\text{ to }10\text{ Hz}$				3	$\mu\text{V}_{PP}$
$e_N$	Input voltage noise density	$R_S = 100\ \Omega, V_I = 0\text{ V}, f = 1\text{ kHz}$ (see Figure 8)				35	$\text{nV}/\sqrt{\text{Hz}}$
<b>INPUT CAPACITANCE</b>							
$Z_{ID}$	Differential				$10 \parallel 0.1$		$\text{M}\Omega \parallel \text{pF}$
$Z_{ICM}$	Common-mode				$4 \parallel 1.5$		$\text{G}\Omega \parallel \text{pF}$
<b>OPEN-LOOP GAIN</b>							
$A_{OL}$	Open-loop voltage gain	$V_S = 15\text{ V}, V_O = 1\text{ V to }11\text{ V}, R_L \geq 2\text{ k}\Omega$ , connected to (V-)			50	100	V/mV
				$T_A = -40^\circ\text{C to }125^\circ\text{C}$	25		
<b>FREQUENCY RESPONSE</b>							
GBW	Gain-bandwidth product	$R_L = 1\text{ M}\Omega, C_L = 20\text{ pF}$ (see Figure 7)				1.2	MHz
SR	Slew rate	$R_L = 1\text{ M}\Omega, C_L = 30\text{ pF}, V_I = \pm 10\text{ V}$ (see Figure 7)				0.5	V/ $\mu\text{s}$
$\theta_m$	Phase margin	$G = +1, R_L = 10\text{ k}\Omega, C_L = 20\text{ pF}$				56	$^\circ$
$t_s$	Settling time	To 0.1%, $V_S = 5\text{ V}, 2\text{-V Step}, G = +1, C_L = 100\text{ pF}$				4	$\mu\text{s}$
	Overload recovery time	$V_{IN} \times \text{gain} > V_S$				10	$\mu\text{s}$
THD+N	Total harmonic distortion + noise	$G = +1, f = 1\text{ kHz}, V_O = 3.53\text{ V}_{RMS}, V_S = 36\text{ V}, R_L = 100\text{ k}\Omega, I_{OUT} \leq 50\ \mu\text{A}, \text{BW} = 80\text{ kHz}$				0.001%	
<b>OUTPUT</b>							
$V_O$	Voltage output swing from rail	Positive Rail (V+)		$I_{OUT} = -50\ \mu\text{A}$	1.35	1.5	V
$V_O$				$I_{OUT} = -1\text{ mA}$	1.4	1.6	V
$V_O$				$I_{OUT} = -5\text{ mA}$	1.5	1.75	V
$V_O$		Negative Rail (V-)		$I_{OUT} = 50\ \mu\text{A}$	100	150	mV
$V_O$				$I_{OUT} = 1\text{ mA}$	0.75	1	V
$V_O$			$V_S = 5\text{ V}, R_L \leq 10\text{ k}\Omega$ connected to (V-)	$T_A = -40^\circ\text{C to }125^\circ\text{C}$	5	20	mV
$I_O$	Output current	Source	$V_S = 15\text{ V}; V_O = V-; V_{ID} = 1\text{ V}$		-20	-30	mA
				$T_A = -40^\circ\text{C to }125^\circ\text{C}$	-10		mA
		Sink	$V_S = 15\text{ V}; V_O = V+; V_{ID} = -1\text{ V}$		10	20	mA
				$T_A = -40^\circ\text{C to }125^\circ\text{C}$	5		mA
		$V_{ID} = -1\text{ V}; V_O = (V-) + 200\text{ mV}$		50	85	$\mu\text{A}$	
$I_{SC}$	Short-circuit current	$V_S = 20\text{ V}, (V+) = 10\text{ V}, (V-) = -10\text{ V}, V_O = 0\text{ V}$			$\pm 40$	$\pm 60$	mA
$C_{LOAD}$	Capacitive load drive				100		pF



## 6.6 Electrical Characteristics - LM2902B and LM2902BA (continued)

For  $V_S = (V_{CC+}) - (V_{CC-}) = 5\text{ V to }36\text{ V}$  ( $\pm 2.5\text{ V to } \pm 18\text{ V}$ ), at  $T_A = 25^\circ\text{C}$ ,  $V_{CM} = V_{OUT} = V_S / 2$ , and  $R_L = 10\text{k}$  connected to  $V_S / 2$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$R_O$	Open-loop output impedance	$f = 1\text{ MHz}, I_O = 0\text{ A}$			300		$\Omega$
<b>POWER SUPPLY</b>							
$I_Q$	Quiescent current per amplifier	$V_S = 5\text{ V}; I_O = 0\text{ A}$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		175	300	$\mu\text{A}$
		$V_S = 36\text{ V}; I_O = 0\text{ A}$	$T_A = -40^\circ\text{C to }125^\circ\text{C}$		350	750	$\mu\text{A}$

## 6.7 Electrical Characteristics for LMx24 and LM324K

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>		$T_A$ <sup>(2)</sup>	LM124, LM224			LM324, LM324K			UNIT			
				MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX				
$V_{IO}$ Input offset voltage	$V_{CC} = 5\text{ V to MAX}$ , $V_{IC} = V_{ICRmin}$ , $V_O = 1.4\text{ V}$		25°C	3		5	3		7	mV			
			Full range			7			9				
$I_{IO}$ Input offset current	$V_O = 1.4\text{ V}$		25°C	2		30	2		50	nA			
			Full range			100			150				
$I_{IB}$ Input bias current	$V_O = 1.4\text{ V}$		25°C	-20		-150	-20		-250	nA			
			Full range			-300			-500				
$V_{ICR}$ Common-mode input voltage range	$V_{CC} = 5\text{ V to MAX}$		25°C	0 to $V_{CC} - 1.5$			0 to $V_{CC} - 1.5$			V			
			Full range	0 to $V_{CC} - 2$			0 to $V_{CC} - 2$						
$V_{OH}$ High-level output voltage	$R_L = 2\text{ k}\Omega$		25°C	$V_{CC} - 1.5$			$V_{CC} - 1.5$			V			
	$V_{CC} = \text{MAX}$		Full range	26		26							
			Full range	27	28	27	28						
$V_{OL}$ Low-level output voltage	$R_L \leq 10\text{ k}\Omega$		Full range	5		20	5		20	mV			
$A_{VD}$ Large-signal differential voltage amplification	$V_{CC+} = 15\text{ V}$ , $V_O = 1\text{ V to } 11\text{ V}$ , $R_L \geq 2\text{ k}\Omega$		25°C	50	100		25	100		V/mV			
			Full range	25		15							
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	70	80		65	80		dB			
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )			25°C	65	100		65	100		dB			
$V_{O1}/V_{O2}$ Crosstalk attenuation	$f = 1\text{ kHz to } 20\text{ kHz}$		25°C	120			120			dB			
$I_O$ Output current	$V_{CC} = 15\text{ V}$ , $V_{ID} = 1\text{ V}$ , $V_O = 0$		Source	25°C	-20		-30	-60	-20		-30	-60	mA
			Full range	-10		-10							
	$V_{CC} = 15\text{ V}$ , $V_{ID} = -1\text{ V}$ , $V_O = 15\text{ V}$		Sink	25°C	10		20		10		20		
			Full range	5		5							
$V_{ID} = -1\text{ V}$ , $V_O = 200\text{ mV}$		25°C	12		30		12		30		$\mu\text{A}$		
$I_{OS}$ Short-circuit output current	$V_{CC}$ at $5\text{ V}$ , $V_O = 0$ , $V_{CC}$ at $-5\text{ V}$		25°C	$\pm 40$		$\pm 60$	$\pm 40$		$\pm 60$	mA			
$I_{CC}$ Supply current (four amplifiers)	$V_O = 2.5\text{ V}$ , no load		Full range	0.7		1.2	0.7		1.2	mA			
	$V_{CC} = \text{MAX}$ , $V_O = 0.5 V_{CC}$ , no load		Full range	1.4		3	1.4		3				

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX  $V_{CC}$  for testing purposes is 26 V for LM2902 and 30 V for the others.
- (2) Full range is  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  for LM124,  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for LM224, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for LM324.
- (3) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.8 Electrical Characteristics for LM2902 and LM2902V

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>		$T_A$ <sup>(2)</sup>	LM2902			LM2902V			UNIT
				MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	
$V_{IO}$ Input offset voltage	$V_{CC} = 5\text{ V to MAX}$ , $V_{IC} = V_{ICRmin}$ , $V_O = 1.4\text{ V}$	Non-A-suffix devices	25°C	3	7		3	7	mV	
			Full range		10		10			
		A-suffix devices	25°C				1	2		
			Full range					4		
$\Delta V_{IO}/\Delta T$ Input offset voltage temperature drift	$R_S = 0\ \Omega$		Full range				7	$\mu\text{V}/^\circ\text{C}$		
$I_{IO}$ Input offset current	$V_O = 1.4\text{ V}$		25°C	2	50		2	50	nA	
			Full range		300		150			
$\Delta I_{IO}/\Delta T$ Input offset voltage temperature drift			Full range				10	$\text{pA}/^\circ\text{C}$		
$I_{IB}$ Input bias current	$V_O = 1.4\text{ V}$		25°C	-20	-250		-20	-250	nA	
			Full range		-500		-500			
$V_{ICR}$ Common-mode input voltage range	$V_{CC} = 5\text{ V to MAX}$		25°C	0 to $V_{CC} - 1.5$		0 to $V_{CC} - 1.5$		V		
			Full range	0 to $V_{CC} - 2$		0 to $V_{CC} - 2$				
$V_{OH}$ High-level output voltage	$R_L = 10\text{ k}\Omega$		25°C	$V_{CC} - 1.5$		$V_{CC} - 1.5$		V		
	$V_{CC} = \text{MAX}$	$R_L = 2\text{ k}\Omega$	Full range	22		26				
		$R_L \geq 10\text{ k}\Omega$	Full range	23	24	27				
$V_{OL}$ Low-level output voltage	$R_L \leq 10\text{ k}\Omega$		Full range	5	20	5	20	mV		
$A_{VD}$ Large-signal differential voltage amplification	$V_{CC} = 15\text{ V}$ , $V_O = 1\text{ V to } 11\text{ V}$ , $R_L \geq 2\text{ k}\Omega$		25°C	25	100	25	100	V/mV		
			Full range	15		15				
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$		25°C	50	80	60	80	dB		
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC}/\Delta V_{IO}$ )			25°C	50	100	60	100	dB		
$V_{O1}/V_{O2}$ Crosstalk attenuation	$f = 1\text{ kHz to } 20\text{ kHz}$		25°C	120		120		dB		
$I_O$ Output current	$V_{CC} = 15\text{ V}$ , $V_{ID} = 1\text{ V}$ , $V_O = 0$	Source	25°C	-20	-30	-60	-20	-30	-60	mA
			Full range	-10		-10				
	$V_{CC} = 15\text{ V}$ , $V_{ID} = -1\text{ V}$ , $V_O = 15\text{ V}$	Sink	25°C	10	20		10	20		
			Full range	5		5				
	$V_{ID} = -1\text{ V}$ , $V_O = 200\text{ mV}$		25°C	30		12	40	$\mu\text{A}$		
$I_{OS}$ Short-circuit output current	$V_{CC}$ at 5 V, $V_O = 0$ , $V_{CC}$ at -5 V		25°C	$\pm 40$	$\pm 60$	$\pm 40$	$\pm 60$	mA		
$I_{CC}$ Supply current (four amplifiers)	$V_O = 2.5\text{ V}$ , no load		Full range	0.7	1.2	0.7	1.2	mA		
	$V_{CC} = \text{MAX}$ , $V_O = 0.5 V_{CC}$ , no load		Full range	1.4	3	1.4	3			

- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified. MAX  $V_{CC}$  for testing purposes is 26 V for LM2902 and 32 V for LM2902V.
- (2) Full range is  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  for LM2902.
- (3) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.9 Electrical Characteristics for LMx24A and LM324KA

at specified free-air temperature,  $V_{CC} = 5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	$T_A$ <sup>(2)</sup>	LM124A			LM224A			LM324A, LM324KA			UNIT
			MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	MIN	TYP <sup>(3)</sup>	MAX	
$V_{IO}$ Input offset voltage	$V_{CC} = 5\text{ V to }30\text{ V}$ , $V_{IC} = V_{ICRmin}$ , $V_O = 1.4\text{ V}$	25°C			2		2	3		2	3	mV
		Full range			4			4			5	
$I_{IO}$ Input offset current	$V_O = 1.4\text{ V}$	25°C			10		2	15		2	30	nA
		Full range			30			30			75	
$I_{IB}$ Input bias current	$V_O = 1.4\text{ V}$	25°C			-50		-15	-80		-15	-100	nA
		Full range			-100			-100			-200	
$V_{ICR}$ Common-mode input voltage range	$V_{CC} = 30\text{ V}$	25°C	0 to		$V_{CC} - 1.5$	0 to		$V_{CC} - 1.5$	0 to		$V_{CC} - 1.5$	V
		Full range	0 to		$V_{CC} - 2$	0 to		$V_{CC} - 2$	0 to		$V_{CC} - 2$	
$V_{OH}$ High-level output voltage	$R_L = 2\text{ k}\Omega$ $V_{CC} = 30\text{ V}$	25°C			$V_{CC} - 1.5$			$V_{CC} - 1.5$			$V_{CC} - 1.5$	V
		Full range	$R_L = 2\text{ k}\Omega$		26		26		26			
			$R_L \geq 10\text{ k}\Omega$		27		27	28		27	28	
$V_{OL}$ Low-level output voltage	$R_L \leq 10\text{ k}\Omega$	Full range			20		5	20		5	20	mV
$A_{VD}$ Large-signal differential voltage amplification	$V_{CC} = 15\text{ V}$ , $V_O = 1\text{ V to }11\text{ V}$ , $R_L \geq 2\text{ k}\Omega$	25°C	50	100		50	100		25	100	V/mV	
		Full range	25			25			15			
CMRR Common-mode rejection ratio	$V_{IC} = V_{ICRmin}$	25°C	70			70	80		65	80	dB	
$k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC} / \Delta V_{IO}$ )		25°C	65			65	100		65	100	dB	
$V_{O1} / V_{O2}$ Crosstalk attenuation	$f = 1\text{ kHz to }20\text{ kHz}$	25°C		120			120			120	dB	
$I_O$ Output current	$V_{CC} = 15\text{ V}$ , $V_{ID} = 1\text{ V}$ , $V_O = 0$	Source	25°C	-20		-20	-30	-60	-20	-30	-60	mA
			Full range	-10		-10			-10			
	$V_{CC} = 15\text{ V}$ , $V_{ID} = -1\text{ V}$ , $V_O = 15\text{ V}$	Sink	25°C	10		10	20		1	20		
			Full range	5		5			5			
	$V_{ID} = -1\text{ V}$ , $V_O = 200\text{ mV}$	25°C	12		12	30		12	30	$\mu\text{A}$		
$I_{OS}$ Short-circuit output current	$V_{CC}$ at 5 V, $V_{CC}$ at -5 V, $V_O = 0$	25°C		$\pm 40$	$\pm 60$		$\pm 40$	$\pm 60$		$\pm 40$	$\pm 60$	mA
$I_{CC}$ Supply current (four amplifiers)	$V_O = 2.5\text{ V}$ , no load	Full range		0.7	1.2		0.7	1.2		0.7	1.2	mA
	$V_{CC} = 30\text{ V}$ , $V_O = 15\text{ V}$ , no load	Full range		1.4	3.		1.4	3		1.4	3	

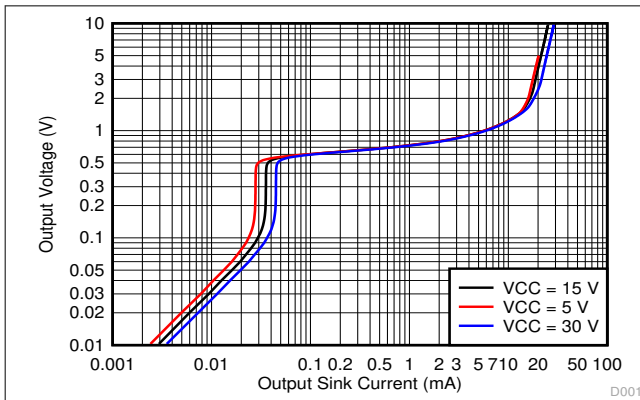
- (1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.  
 (2) Full range is  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  for LM124A,  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$  for LM224A, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for LM324A.  
 (3) All typical values are at  $T_A = 25^\circ\text{C}$ .

## 6.10 Operating Conditions

$V_{CC} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

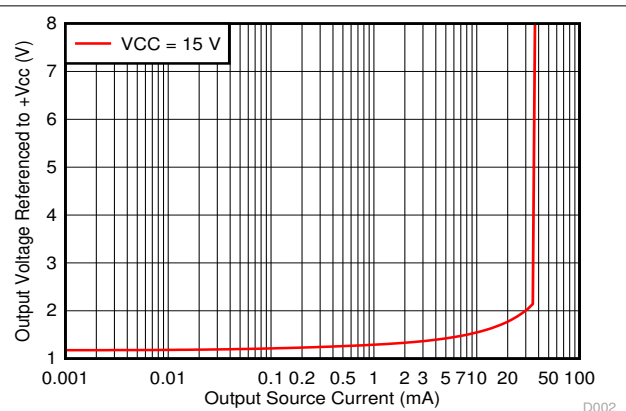
PARAMETER	TEST CONDITIONS	TYP	UNIT
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$ , $C_L = 30\text{ pF}$ , $V_I = \pm 10\text{ V}$ (see Figure 7-1)	0.5	$\text{V}/\mu\text{s}$
$B_1$ Unity-gain bandwidth	$R_L = 1\text{ M}\Omega$ , $C_L = 20\text{ pF}$ (see Figure 7-1)	1.2	MHz
$V_n$ Equivalent input noise voltage	$R_S = 100\ \Omega$ , $V_I = 0\text{ V}$ , $f = 1\text{ kHz}$ (see Figure 7-2)	35	$\text{nV}/\sqrt{\text{Hz}}$

## 6.11 Typical Characteristics: All Devices Except B and BA versions



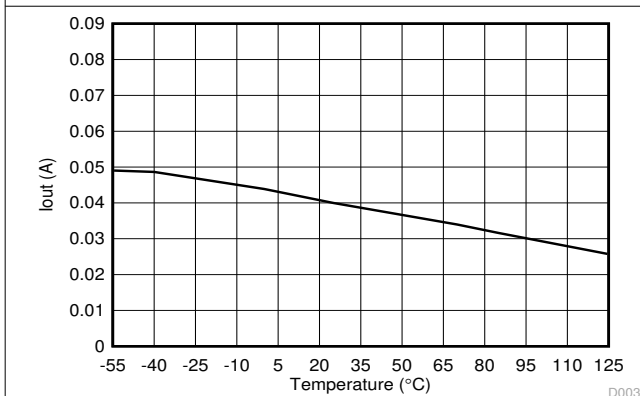
**Figure 6-1. Output Sinking Characteristics**

D001



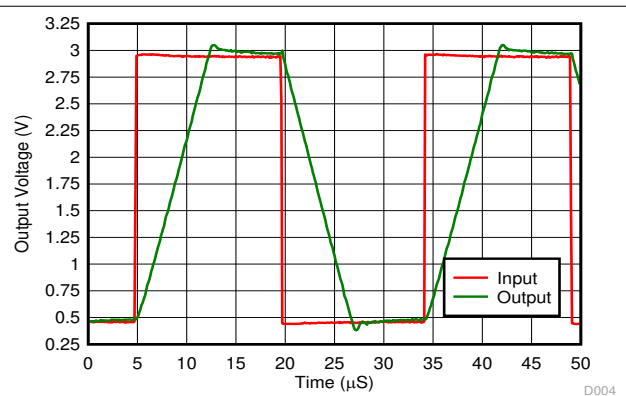
**Figure 6-2. Output Sourcing Characteristics**

D002



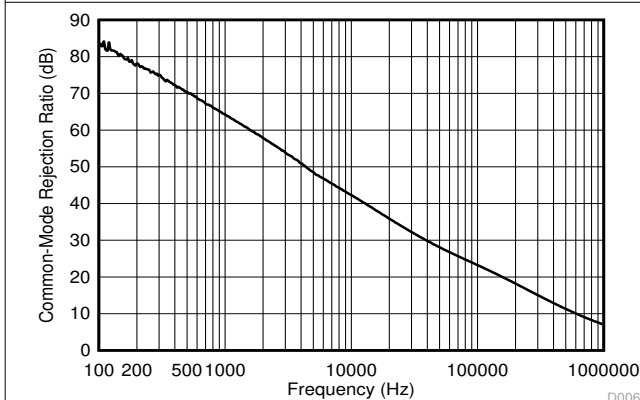
**Figure 6-3. Source Current Limiting**

D003



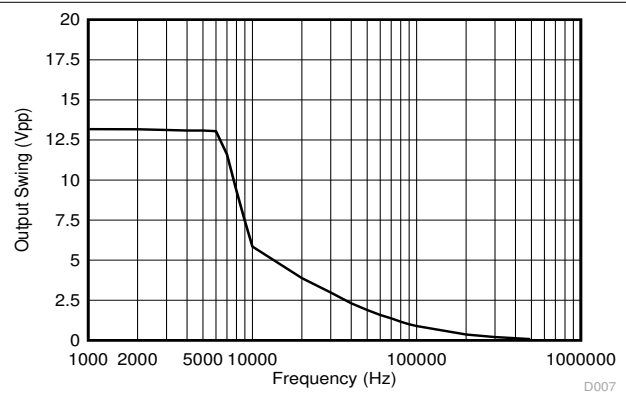
**Figure 6-4. Voltage Follower Large Signal Response (50 pF)**

D004



**Figure 6-5. Common-Mode Rejection Ratio**

D006



**Figure 6-6. Maximum Output Swing vs. Frequency (VCC = 15 V)**

D007

## 7 Parameter Measurement Information

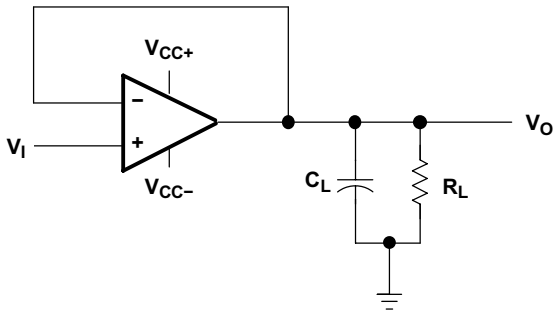


Figure 7-1. Unity-Gain Amplifier

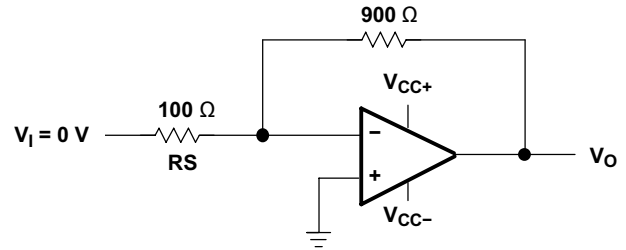


Figure 7-2. Noise-Test Circuit

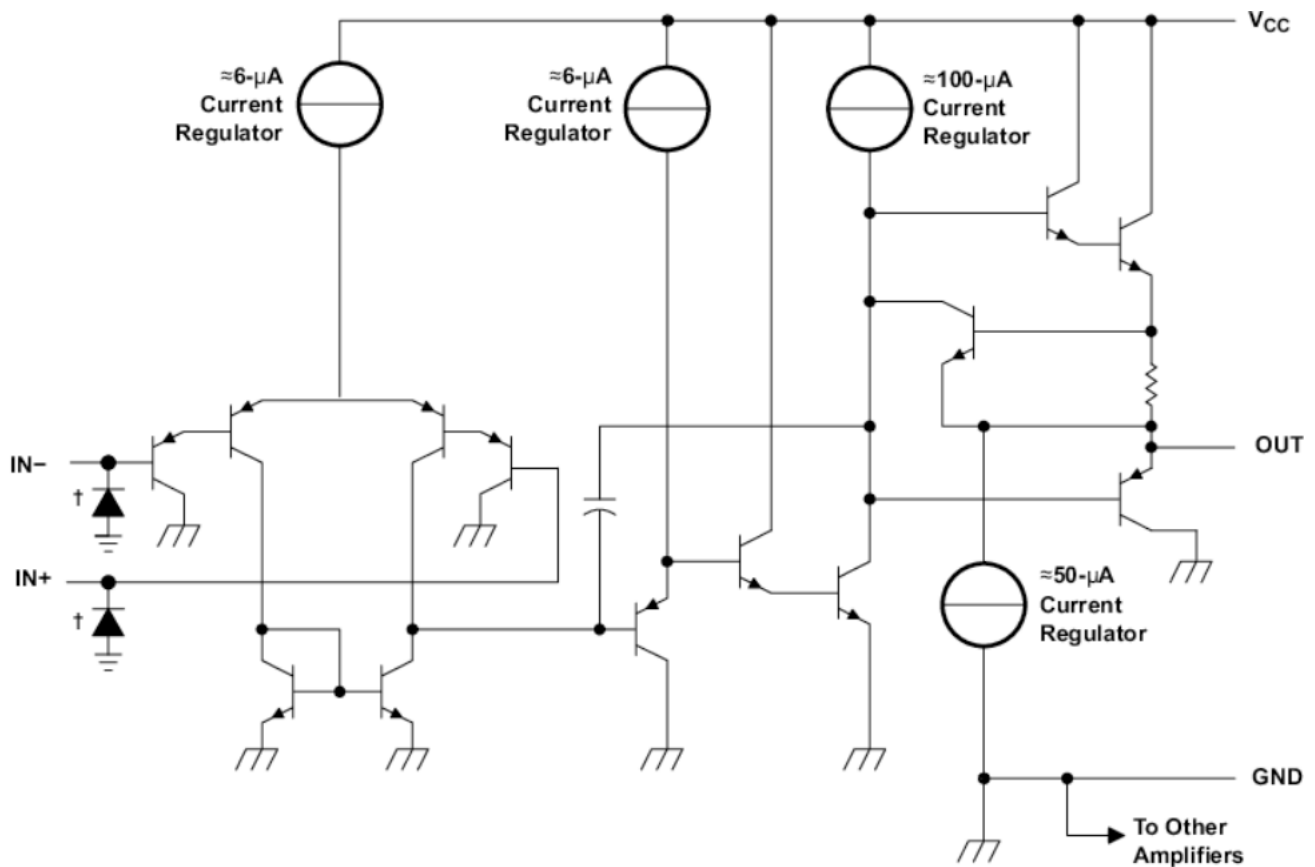
## 8 Detailed Description

### 8.1 Overview

These devices consist of four independent high-gain frequency-compensated operational amplifiers that are designed specifically to operate from a single supply over a wide range of voltages. Operation from split supplies also is possible if the difference between the two supplies is 3 V to 36 V (B and BA versions), 3 V to 26 V (for LM2902 devices) or 3 V to 30V (for all other devices), and  $V_{CC}$  is at least 1.5 V more positive than the input common-mode voltage. The low supply-current drain is independent of the magnitude of the supply voltage.

Applications include transducer amplifiers, DC amplification blocks, and all the conventional operational-amplifier circuits that now can be more easily implemented in single-supply-voltage systems. For example, the LM124 device can be operated directly from the standard 5-V supply that is used in digital systems and provides the required interface electronics, without requiring additional  $\pm 15$ -V supplies.

### 8.2 Functional Block Diagram



COMPONENT COUNT (total device)	
Epi-FET	1
Transistors	95
Diodes	4
Resistors	11
Capacitors	4

ESD protection cells - available on B, BA, and K versions only

## 8.3 Feature Description

### 8.3.1 Unity-Gain Bandwidth

Gain bandwidth product is found by multiplying the measured bandwidth of an amplifier by the gain at which that bandwidth was measured. These devices have a high gain bandwidth of 1.2 MHz.

### 8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. These devices have a 0.5-V/ $\mu$ s slew rate.

### 8.3.3 Input Common Mode Range

The valid common mode range is from device ground to  $V_{CC} - 1.5$  V ( $V_{CC} - 2$  V across temperature). Inputs may exceed  $V_{CC}$  up to the maximum  $V_{CC}$  without device damage. At least one input must be in the valid input common mode range for output to be correct phase. If both inputs exceed valid range then output phase is undefined. If either input is less than  $-0.3$  V then input current should be limited to 1 mA and output phase is undefined.

## 8.4 Device Functional Modes

These devices are powered on when the supply is connected. This device can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.



## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The LMx24 and LM2902 operational amplifiers are useful in a wide range of signal conditioning applications. Inputs can be powered before VCC for flexibility in multiple supply circuits.

### 9.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes it a negative voltage of the same magnitude. In the same manner, it also makes negative voltages positive.

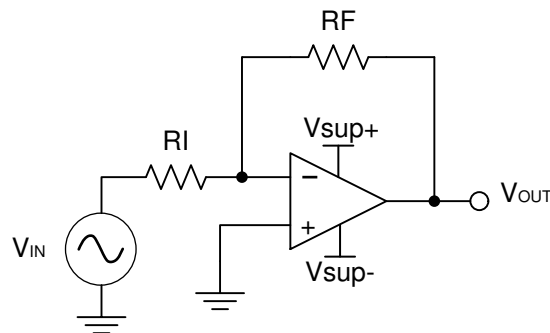


Figure 9-1. Application Schematic

#### 9.2.1 Design Requirements

The supply voltage must be chosen such that it is larger than the input voltage range and output range. For instance, this application will scale a signal of  $\pm 0.5$  V to  $\pm 1.8$  V. Setting the supply at  $\pm 12$  V is sufficient to accommodate this application.

#### 9.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using [Equation 1](#) and [Equation 2](#):

$$A_v = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_v = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Once the desired gain is determined, choose a value for  $R_I$  or  $R_F$ . Choosing a value in the kilohm range is desirable because the amplifier circuit will use currents in the milliamp range. This ensures the part will not draw too much current. This example will choose 10 k $\Omega$  for  $R_I$  which means 36 k $\Omega$  will be used for  $R_F$ . This was determined by [Equation 3](#).

$$A_v = -\frac{R_F}{R_I} \quad (3)$$

### 9.2.3 Application Curve

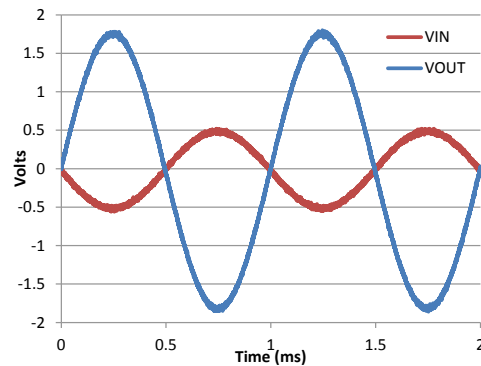


Figure 9-2. Input and Output Voltages of the Inverting Amplifier

## 10 Power Supply Recommendations

### CAUTION

Supply voltages larger than 32 V for a single supply, or outside the range of  $\pm 16$  V for a dual supply can permanently damage the device (see the [Section 6.1](#)).

Place 0.1- $\mu$ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the [Section 11](#).

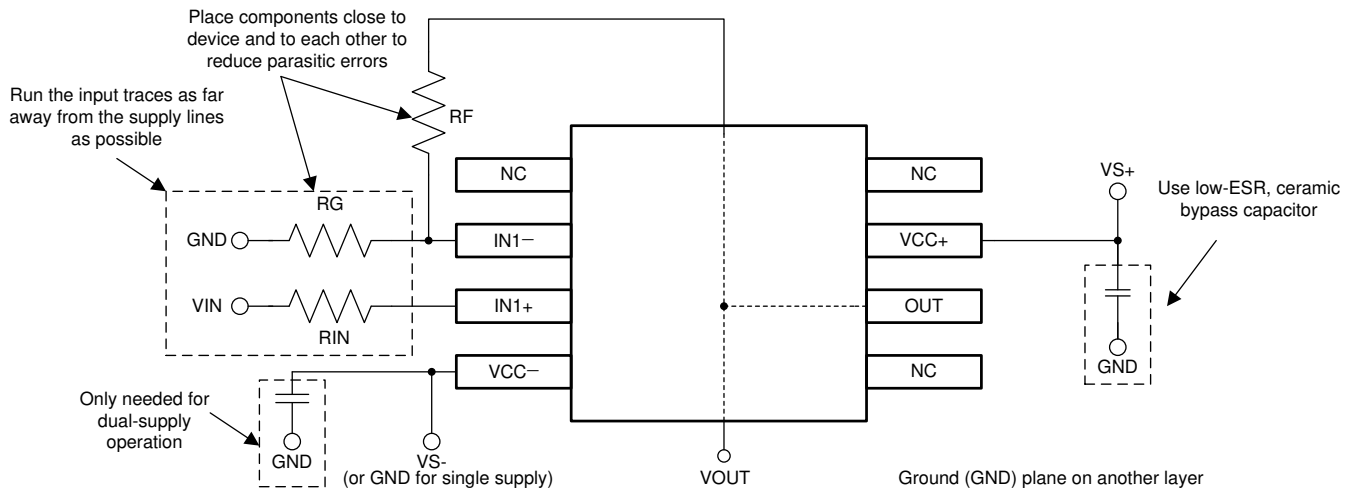
## 11 Layout

### 11.1 Layout Guidelines

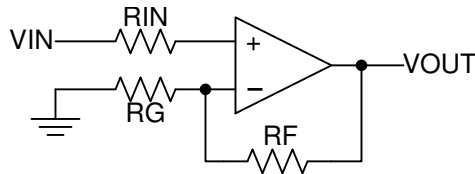
For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in [Section 11.2](#).
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

## 11.2 Layout Examples



**Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration**



**Figure 11-2. Operational Amplifier Schematic for Noninverting Configuration**

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
All trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-7704301VCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-7704301VC A LM124JQMLV	<a href="#">Samples</a>
5962-9950403V9B	ACTIVE	XCEPT	KGD	0	100	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 125		<a href="#">Samples</a>
5962-9950403VCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9950403VC A LM124AJQMLV	<a href="#">Samples</a>
77043012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	77043012A LM124FKB	<a href="#">Samples</a>
7704301CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704301CA LM124JB	<a href="#">Samples</a>
7704301DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704301DA LM124WB	<a href="#">Samples</a>
77043022A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	77043022A LM124AFKB	<a href="#">Samples</a>
7704302CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704302CA LM124AJB	<a href="#">Samples</a>
7704302DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704302DA LM124AWB	<a href="#">Samples</a>
JM38510/11005BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11005BCA	<a href="#">Samples</a>
LM124AFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	77043022A LM124AFKB	<a href="#">Samples</a>
LM124AJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM124AJ	<a href="#">Samples</a>
LM124AJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704302CA LM124AJB	<a href="#">Samples</a>
LM124AWB	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704302DA LM124AWB	<a href="#">Samples</a>
LM124D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	<a href="#">Samples</a>
LM124DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM124DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	<a href="#">Samples</a>
LM124DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM124	<a href="#">Samples</a>
LM124FKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	77043012A LM124FKB	<a href="#">Samples</a>
LM124J	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM124J	<a href="#">Samples</a>
LM124JB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704301CA LM124JB	<a href="#">Samples</a>
LM124W	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	LM124W	<a href="#">Samples</a>
LM124WB	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	7704301DA LM124WB	<a href="#">Samples</a>
LM224AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224A	<a href="#">Samples</a>
LM224ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-25 to 85	LM224A	<a href="#">Samples</a>
LM224ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224A	<a href="#">Samples</a>
LM224ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224A	<a href="#">Samples</a>
LM224AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224AN	<a href="#">Samples</a>
LM224D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224	<a href="#">Samples</a>
LM224DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224	<a href="#">Samples</a>
LM224DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-25 to 85	LM224	<a href="#">Samples</a>
LM224DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LM224	<a href="#">Samples</a>
LM224DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224	<a href="#">Samples</a>
LM224KAD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	<a href="#">Samples</a>
LM224KADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	<a href="#">Samples</a>
LM224KADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM224KADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224KA	<a href="#">Samples</a>
LM224KAN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224KAN	<a href="#">Samples</a>
LM224KDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM224K	<a href="#">Samples</a>
LM224KDRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	-25 to 85		<a href="#">Samples</a>
LM224KN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224KN	<a href="#">Samples</a>
LM224N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224N	<a href="#">Samples</a>
LM224NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	LM224N	<a href="#">Samples</a>
LM2902D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	<a href="#">Samples</a>
LM2902DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LM2902	<a href="#">Samples</a>
LM2902DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	<a href="#">Samples</a>
LM2902DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2902	<a href="#">Samples</a>
LM2902DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	<a href="#">Samples</a>
LM2902KAVQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	<a href="#">Samples</a>
LM2902KAVQDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	<a href="#">Samples</a>
LM2902KAVQPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	<a href="#">Samples</a>
LM2902KAVQPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KA	<a href="#">Samples</a>
LM2902KD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	<a href="#">Samples</a>
LM2902KDB	ACTIVE	SSOP	DB	14	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	<a href="#">Samples</a>
LM2902KDG4	ACTIVE	SOIC	D	14	50	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
LM2902KDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	<a href="#">Samples</a>
LM2902KN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2902KN	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2902KNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	<a href="#">Samples</a>
LM2902KNSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902K	<a href="#">Samples</a>
LM2902KPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	<a href="#">Samples</a>
LM2902KPWE4	ACTIVE	TSSOP	PW	14	90	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>
LM2902KPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902K	<a href="#">Samples</a>
LM2902KVQDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	<a href="#">Samples</a>
LM2902KVQDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	<a href="#">Samples</a>
LM2902KVQPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	<a href="#">Samples</a>
LM2902KVQPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902KV	<a href="#">Samples</a>
LM2902N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU   SN	N / A for Pkg Type	-40 to 125	LM2902N	<a href="#">Samples</a>
LM2902NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2902N	<a href="#">Samples</a>
LM2902NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM2902	<a href="#">Samples</a>
LM2902PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902	<a href="#">Samples</a>
LM2902PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	L2902	<a href="#">Samples</a>
LM2902PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902	<a href="#">Samples</a>
LM2902PWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L2902	<a href="#">Samples</a>
LM2902PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2902	<a href="#">Samples</a>
LM324AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	<a href="#">Samples</a>
LM324ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	<a href="#">Samples</a>
LM324ADE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	<a href="#">Samples</a>
LM324ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	LM324A	<a href="#">Samples</a>



Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM324ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	<a href="#">Samples</a>
LM324ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	<a href="#">Samples</a>
LM324AN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM324AN	<a href="#">Samples</a>
LM324ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	<a href="#">Samples</a>
LM324ANSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324A	<a href="#">Samples</a>
LM324APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324A	<a href="#">Samples</a>
LM324APWE4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324A	<a href="#">Samples</a>
LM324APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	L324A	<a href="#">Samples</a>
LM324APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324A	<a href="#">Samples</a>
LM324D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324DE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324DG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324DRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324KAD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	<a href="#">Samples</a>
LM324KADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	<a href="#">Samples</a>
LM324KADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	<a href="#">Samples</a>
LM324KAN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM324KAN	<a href="#">Samples</a>
LM324KANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324KA	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM324KAPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324KA	<a href="#">Samples</a>
LM324KAPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324KA	<a href="#">Samples</a>
LM324KAPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324KA	<a href="#">Samples</a>
LM324KDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324K	<a href="#">Samples</a>
LM324KN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM324KN	<a href="#">Samples</a>
LM324KNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324K	<a href="#">Samples</a>
LM324KPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324K	<a href="#">Samples</a>
LM324KPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324K	<a href="#">Samples</a>
LM324N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU   SN	N / A for Pkg Type	0 to 70	LM324N	<a href="#">Samples</a>
LM324NE3	ACTIVE	PDIP	N	14	25	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 70	LM324N	<a href="#">Samples</a>
LM324NE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM324N	<a href="#">Samples</a>
LM324NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324NSRE4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324NSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LM324	<a href="#">Samples</a>
LM324PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324	<a href="#">Samples</a>
LM324PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	0 to 70	L324	<a href="#">Samples</a>
LM324PWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324	<a href="#">Samples</a>
LM324PWRG3	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L324	<a href="#">Samples</a>
LM324PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L324	<a href="#">Samples</a>
M38510/11005BCA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11005BCA	<a href="#">Samples</a>
PLM2902BIPWR	ACTIVE	TSSOP	PW	14	3000	TBD	Call TI	Call TI	-40 to 125		<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLM324BIPWR	ACTIVE	TSSOP	PW	14	3000	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LM124, LM124-SP, LM124M, LM2902, LM2902B :**

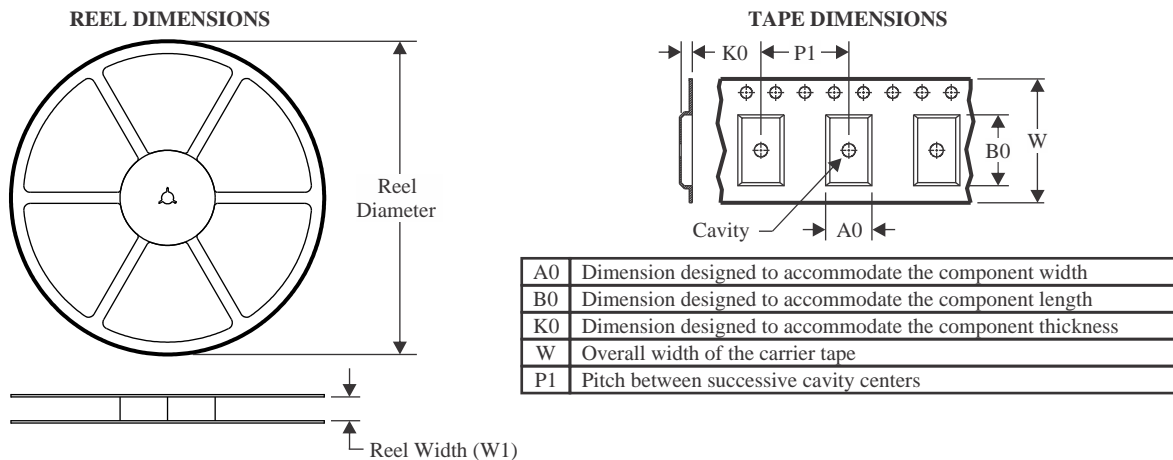
- Catalog : [LM124](#), [LM124](#)

- Automotive : [LM2902-Q1](#), [LM2902B-Q1](#)
- Enhanced Product : [LM2902-EP](#)
- Military : [LM124M](#), [LM124M](#)
- Space : [LM124-SP](#), [LM124-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM124DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM224ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM224DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224DRG3	SOIC	D	14	2500	330.0	17.5	6.4	9.05	2.1	8.0	16.0	Q1
LM224DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM224DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224KADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM224KADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM2902DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2902DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902KAVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KAVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM2902KNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM2902KPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902KVQPWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM2902PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM324ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324ADR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM324ADRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324DR	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM324DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324DRG3	SOIC	D	14	2500	330.0	17.5	6.4	9.05	2.1	8.0	16.0	Q1
LM324DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
LM324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324KAPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324KDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
LM324KNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324KPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
LM324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324PWRG3	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
LM324PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

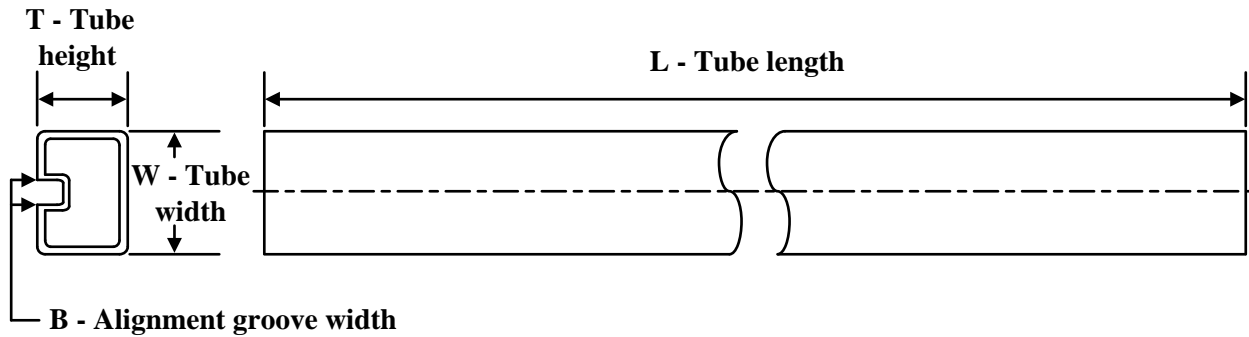
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM124DR	SOIC	D	14	2500	350.0	350.0	43.0
LM224ADR	SOIC	D	14	2500	356.0	356.0	35.0
LM224ADR	SOIC	D	14	2500	364.0	364.0	27.0
LM224ADRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM224ADRG4	SOIC	D	14	2500	340.5	336.1	32.0
LM224DR	SOIC	D	14	2500	364.0	364.0	27.0
LM224DR	SOIC	D	14	2500	356.0	356.0	35.0
LM224DRG3	SOIC	D	14	2500	333.2	345.9	28.6
LM224DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM224DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM224KADR	SOIC	D	14	2500	356.0	356.0	35.0
LM224KDR	SOIC	D	14	2500	356.0	356.0	35.0
LM2902DR	SOIC	D	14	2500	340.5	336.1	32.0
LM2902DR	SOIC	D	14	2500	364.0	364.0	27.0
LM2902DR	SOIC	D	14	2500	356.0	356.0	35.0
LM2902DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM2902DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM2902DRG4	SOIC	D	14	2500	340.5	336.1	32.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2902KAVQPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902KAVQPWRG4	TSSOP	PW	14	2000	367.0	367.0	35.0
LM2902KDR	SOIC	D	14	2500	356.0	356.0	35.0
LM2902KNSR	SO	NS	14	2000	356.0	356.0	35.0
LM2902KPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902KVQPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902KVQPWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902NSR	SO	NS	14	2000	356.0	356.0	35.0
LM2902PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM2902PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM2902PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM2902PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
LM324ADR	SOIC	D	14	2500	356.0	356.0	35.0
LM324ADR	SOIC	D	14	2500	364.0	364.0	27.0
LM324ADRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM324ANSR	SO	NS	14	2000	356.0	356.0	35.0
LM324APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM324APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324DR	SOIC	D	14	2500	364.0	364.0	27.0
LM324DR	SOIC	D	14	2500	356.0	356.0	35.0
LM324DRG3	SOIC	D	14	2500	333.2	345.9	28.6
LM324DRG3	SOIC	D	14	2500	364.0	364.0	27.0
LM324DRG4	SOIC	D	14	2500	340.5	336.1	32.0
LM324DRG4	SOIC	D	14	2500	356.0	356.0	35.0
LM324KADR	SOIC	D	14	2500	356.0	356.0	35.0
LM324KANSR	SO	NS	14	2000	356.0	356.0	35.0
LM324KAPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324KDR	SOIC	D	14	2500	356.0	356.0	35.0
LM324KNSR	SO	NS	14	2000	356.0	356.0	35.0
LM324KPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324NSR	SO	NS	14	2000	356.0	356.0	35.0
LM324PWR	TSSOP	PW	14	2000	364.0	364.0	27.0
LM324PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
LM324PWRG3	TSSOP	PW	14	2000	364.0	364.0	27.0
LM324PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9950403VCA	J	CDIP	14	1	506.98	15.24	13440	NA
77043012A	FK	LCCC	20	1	506.98	12.06	2030	NA
7704301DA	W	CFP	14	1	506.98	26.16	6220	NA
77043022A	FK	LCCC	20	1	506.98	12.06	2030	NA
7704302DA	W	CFP	14	1	506.98	26.16	6220	NA
LM124AFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
LM124AWB	W	CFP	14	1	506.98	26.16	6220	NA
LM124D	D	SOIC	14	50	505.46	6.76	3810	4
LM124DG4	D	SOIC	14	50	505.46	6.76	3810	4
LM124FKB	FK	LCCC	20	1	506.98	12.06	2030	NA
LM124W	W	CFP	14	1	506.98	26.16	6220	NA
LM124WB	W	CFP	14	1	506.98	26.16	6220	NA
LM224AD	D	SOIC	14	50	506.6	8	3940	4.32
LM224AN	N	PDIP	14	25	506	13.97	11230	4.32
LM224D	D	SOIC	14	50	506.6	8	3940	4.32
LM224DG4	D	SOIC	14	50	506.6	8	3940	4.32
LM224KAD	D	SOIC	14	50	506.6	8	3940	4.32
LM224KADG4	D	SOIC	14	50	506.6	8	3940	4.32
LM224KAN	N	PDIP	14	25	506	13.97	11230	4.32
LM224KN	N	PDIP	14	25	506	13.97	11230	4.32
LM224N	N	PDIP	14	25	506	13.97	11230	4.32
LM224NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM2902D	D	SOIC	14	50	506.6	8	3940	4.32
LM2902KD	D	SOIC	14	50	506.6	8	3940	4.32
LM2902KDB	DB	SSOP	14	80	530	10.5	4000	4.1
LM2902KN	N	PDIP	14	25	506	13.97	11230	4.32
LM2902KPW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM2902N	N	PDIP	14	25	506	13.97	11230	4.32
LM2902N	N	PDIP	14	25	506.1	9	600	5.4

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2902NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM2902PW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM324AD	D	SOIC	14	50	506.6	8	3940	4.32
LM324ADE4	D	SOIC	14	50	506.6	8	3940	4.32
LM324AN	N	PDIP	14	25	506	13.97	11230	4.32
LM324AN	N	PDIP	14	25	506	13.97	11230	4.32
LM324APW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM324APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
LM324D	D	SOIC	14	50	506.6	8	3940	4.32
LM324D	D	SOIC	14	50	507	8	3940	4.32
LM324DE4	D	SOIC	14	50	507	8	3940	4.32
LM324DE4	D	SOIC	14	50	506.6	8	3940	4.32
LM324DG4	D	SOIC	14	50	507	8	3940	4.32
LM324DG4	D	SOIC	14	50	506.6	8	3940	4.32
LM324KAD	D	SOIC	14	50	506.6	8	3940	4.32
LM324KAN	N	PDIP	14	25	506	13.97	11230	4.32
LM324KAN	N	PDIP	14	25	506	13.97	11230	4.32
LM324KAPW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM324KN	N	PDIP	14	25	506	13.97	11230	4.32
LM324KN	N	PDIP	14	25	506	13.97	11230	4.32
LM324KPW	PW	TSSOP	14	90	530	10.2	3600	3.5
LM324N	N	PDIP	14	25	506	13.97	11230	4.32
LM324N	N	PDIP	14	25	506.1	9	600	5.4
LM324N	N	PDIP	14	25	506	13.97	11230	4.32
LM324NE3	N	PDIP	14	25	506.1	9	600	5.4
LM324NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM324NE4	N	PDIP	14	25	506	13.97	11230	4.32
LM324PW	PW	TSSOP	14	90	530	10.2	3600	3.5

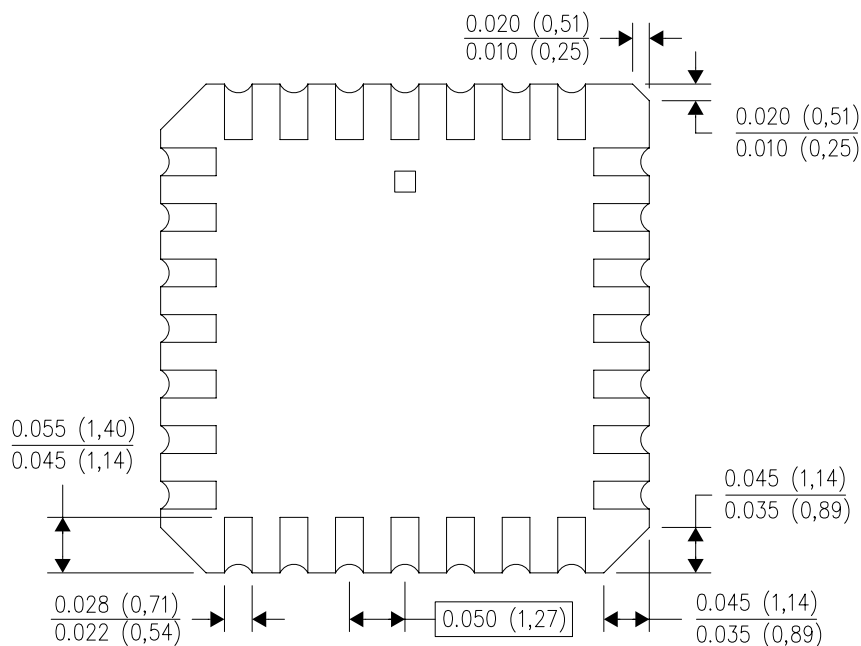
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F14

J 14

**GENERIC PACKAGE VIEW**  
**CDIP - 5.08 mm max height**  
CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040083-5/G

J0014A



# PACKAGE OUTLINE

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

**NOTES:**

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

# EXAMPLE BOARD LAYOUT

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE: 5X



4214771/A 05/2017





D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

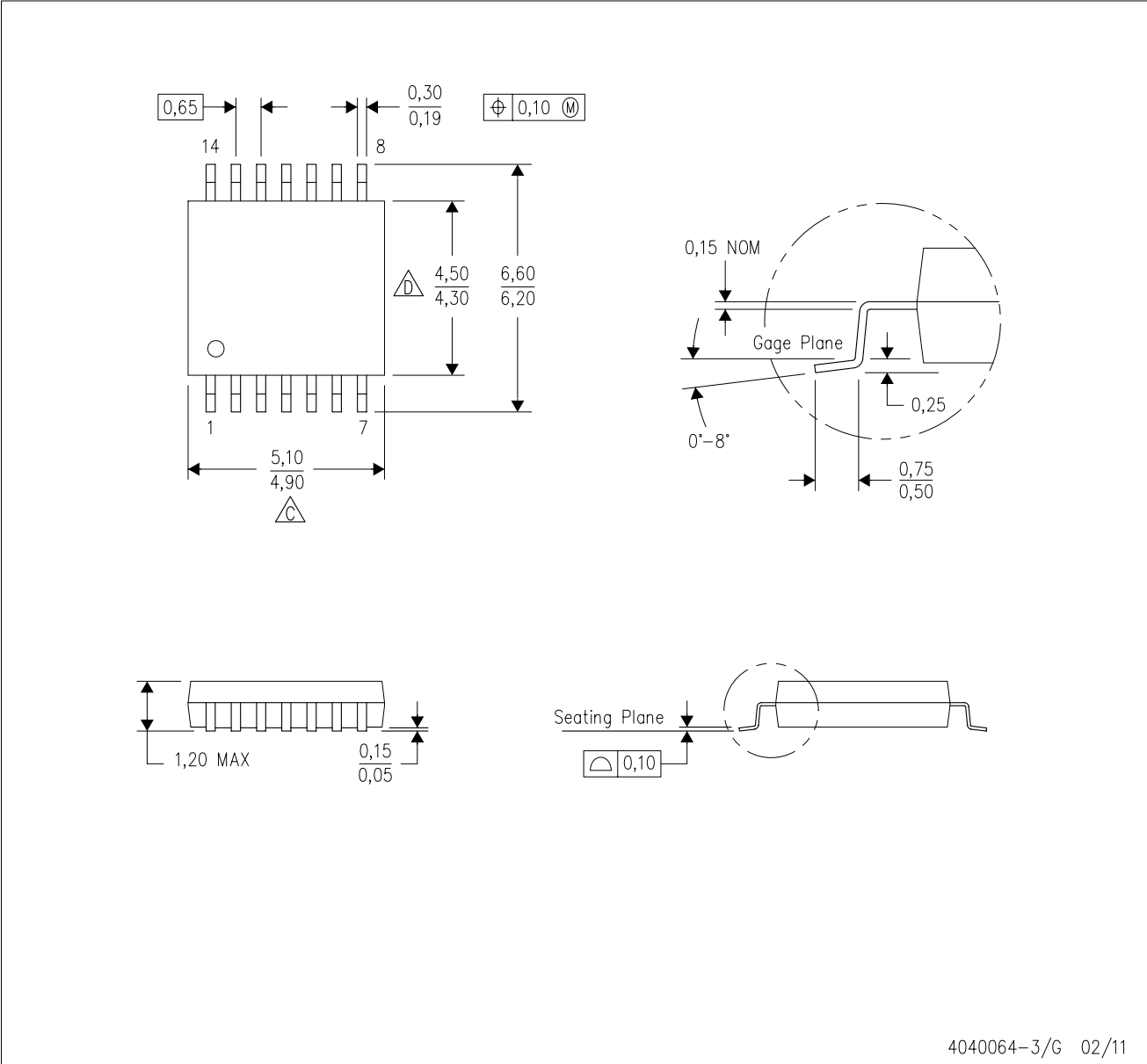


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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